GRS Gamma Analog Commands
(Brassboard FPGA)

Hex Command Id [15:8]	Hex Data Range [7:0]	Command Function	Notes
00	00	NOP	No Operation Command .
00	0A	Cmd_Reject Reset	Resets the command reject flag.
00	AA	Cmd_Counter Reset	Resets the command counter.
01	01	APPS Board Reset	Resets the APPS logic.
10	00 - FF	DAC 0 Level	LLD Threshold DAC.
11	00 – FF	DAC 1 Level	L1 Threshold DAC.
12	00 – FF	DAC 2 Level	L2 Threshold DAC.
13	00 – FF	DAC 3 Level	L3 Threshold DAC.
14	00 – FF	DAC 4 Level	ULD Threshold DAC.
15	00 – FF	DAC 5 Level	Spare channel in brassboard.
16	00 – FF	DAC 6 Level	Spare channel in brassboard.
17	00 - FF	DAC 7 Level	HVBS DAC (00 – FF -> 0V to 5000V)
18	01	DAC Clear All Command	Command bits [7:0] not used by cmd processor.
20	00 – FF	Shaping Amplifier Gain Control	Gain range ~ 4 MeV to 16 MeV over F.S. range
28	00 – 1F	Analog HK Mux Channel	Bits [7:5] are unused by command processor.
2A	00 - FF	HK Telemetry Command	Bits [3:0] set the digital multiplexer position. Bit [7] == 1 initiates a digital HK telemetry word transfer to the CEB. One telemetry word per cmd. Bit [7] == 0 changes the digital mux position but does not initiate a data transfer. Bits [6:4] are unused by command processor.
2B	00 or 01	Test Pulser Command	Bit [0] == 0 => test pulser is disabled. Bit [0] == 1 => test pulser is enabled. Bits [7:1] are unused by command processor
2C	00 or 01	PHA Logic Command	Bit [0] == 0 => Nominal (enabled) PHA mode. Bit [0] == 1 => PHA stop/abort mode. Bits [7:1] are unused by command processor
2D	00 or 01	High Voltage Command	Bit [0] == 0 => HVBS disabled; output voltage driven of supply driven to ground. Bit [0] == 1 => HVBS enabled (DAC enabled, HVBS oscillator on). Bits [2:1] are latched into memory, but are otherwise unused in the brassboard. Bits [7:3] are unused by command processor
2E, 2F	--	Spare Commands	Not implemented in brassboard rev. of Actel. Pattern reserved for possible future use. Will be rejected on APPS brassboard.
Others	--	Invalid Commands	Should initiate a command reject flag.

Useful Diagnostic/Checkout Command Sequences:

(1) Ability to send all valid commands individually with command mneumonics.

(2) Ability to send the NOP command in a loop (i.e. once per second, once per millisecond, or something similar)

(3) Looping DAC 5 command – single value (using DAC 5 as a diagnostic)

(4) Looping DAC 5 command – through values 00 - FF (using DAC 5 as a diagnostic)

(5) Digital HK readout macro: reads through all 16 digital housekeeping channels and stores contents to memory. A display of the APPS "digital status" would be useful.

(6) Analog HK readout macro: reads through all 32 analog housekeeping channels, completes the conversion, and stores the converted data. A display of the APPS "analog HK status" would be useful.

(7) Ability to send an invalid command, such as 'h30, to verify invalid commands are rejected.

(8) A telemetry page with the raw APPS hex data may be useful as well as the scaled/converted values.

GRS Gamma Analog Digital HK Telemetry Words
(Brassboard FPGA)

Dig HK Id [15:14]	Mux Chan Id [13:10]	Data Bits [9:0]
11	0 x 0	{ Cmd_Mach[3:0], Cmd_Data[5:0] }
11	0 x 1	{ DAC 0 Level [7:0], DAC 1 Level [7:6] }
11	0 x 2	{ DAC 1 Level [5:0], DAC 2 Level [7:4] }
11	0 x 3	{ DAC 2 Level [3:0], DAC 3 Level [7:2] }
11	0 x 4	{ DAC 3 Level [1:0], DAC 4 Level [7:0] }
11	0 x 5	{ DAC 5 Level [7:0], DAC 6 Level [7:6] }
11	0 x 6	{ DAC 6 Level [5:0], DAC 7 Level [7:4] }
11	0 x 7	{ DAC 7 Level [3:0], BPHA [15:10] }
11	0 x 8	{ BPHA [9:0] }
11	0 x 9	{ TP_Mach[3:0], TP_Enable, Cmd_Accept, Cmd_Reject, Pha_latch, Load_mem, APPS_Reset }
11	0 x A	{ Reset, Telem_Mach[2:0], Analog Multiplexer Channel [5:0] }
11	0 x B	{ Cmd_Mach[3:0], Telem_Mach[2:0], HV_Cmds[2:1], HV_Enable }
11	0 x C	{ Cmd_Mach[3:2], Cmd_Data[15:8] }
11	0 x D	{ Cmd_Mach[3:2], Cmd_Data[7:0] }
11	0 x E	{ Cmd_Mach[3:2], Command Counter [7:0] }
11	0 x F	{ Cmd_Mach[3:2], Shaping Amp Gain [7:0] }

GRS Gamma Analog HK Multiplexer
(Brassboard APPS)

Mux Chan Id	Analog Parameter	Slope	Offset	Notes
0 x 0	Electrometer, Fast	1V / nA	TBD mV	Detector Leakage Current Monitor, direct
0 x 1	Electrometer, Slow	1V / nA	TBD mV	Detector Leakage Current Monitor, filtered
0 x 2	APPS VCC	0.417 V/ V	TBD mV	Gamma Analog +12V voltage monitor
0 x 3	APPS ICC	50 mV/ mA	TBD mV	Gamma Analog +12V current monitor
0 x 4	APPS VSS	0.417 V/ V	TBD mV	Gamma Analog -12V voltage monitor
0 x 5	APPS ISS	50 mV/ mA	TBD mV	Gamma Analog -12V current monitor
0 x 6	APPS VDD	1 V/ V	TBD mV	Gamma Analog +5V voltage monitor
0 x 7	APPS IDD	100 mV/ mA	TBD mV	Gamma Analog +5V current monitor
0 x 8	HVBS ICC	100 mV/ mA	TBD mV	High Voltage Bias Supply +12V current monitor
0 x 9	HVBS ISS	100 mV/ mA	TBD mV	High Voltage Bias Supply -12V current monitor
0 x A	GPA ICC	50 mV/ mA	TBD mV	Gamma Pulse Amplifier +12V current monitor
0 x B	GPA ISS	50 mV/ mA	TBD mV	Gamma Pulse Amplifier -12V current monitor
0 x C	VDD	1 V/ V	0	VDD direct monitor @ 5V (~2V)
0 x D	1.66V Ref	1 V/ V	0	Fixed Ref Voltage @ 1.666 V (~ -1.333 V)
0 x E	3.33V Ref	1 V/ V	0	Fixed Ref Voltage @ 3.333 V (~ 0.333 V)
0 x F	5.00V Ref	1 V/ V	0	Fixed Ref Voltage @ 5.000 V (~ 2.000 V)
0 x 10	DAC 0 Monitor	1 V/ V	TBD mV	Range 0 – 5V (~ -3V to +2V)
0 x 11	DAC 1 Monitor	1 V/ V	TBD mV	Range 0 – 5V (~ -3V to +2V)
0 x 12	DAC 2 Monitor	1 V/ V	TBD mV	Range 0 – 5V (~ -3V to +2V)
0 x 13	DAC 3 Monitor	1 V/ V	TBD mV	Range 0 – 5V (~ -3V to +2V)
0 x 14	DAC 4 Monitor	1 V/ V	TBD mV	Range 0 – 5V (~ -3V to +2V)
0 x 15	DAC 5 Monitor	1 V/ V	TBD mV	Range 0 – 5V (~ -3V to +2V)
0 x 16	DAC 6 Monitor	1 V/ V	TBD mV	Range 0 – 5V (~ -3V to +2V)
0 x 17	DAC 7 Monitor	1 V/ V	TBD mV	Range 0 – 5V (~ -3V to +2V)
0 x 18	HVBS Output Monitor	1 V/ V	TBD mV	Range 0 – 5V (~ -3V to +2V)
0 x 19	0V	1 V/ V	0	Spare
0 x 1A	HVBS Enable Monitor	1 V/ V	TBD mV	Range 0 – 5V (~ -3V to +2V)
0 x 1B	APPS1 Vref Temp	12.8 mV/ °C	25 mV	Range 0 – 6V (~ -3V to +3V)
0 x 1C	GPA Temp	-10 mV/ °C	TBD mV	Range 0 – 6V (~ -3V to +3V)
0 x 1D	HVBS Temp	-10 mV/ °C	TBD mV	Range 0 – 6V (~ -3V to +3V)
0 x 1E	0V	1 V/ V	0	Spare
0 x 1F	Mux Offset	1 V/ V	0	Brassboard = 0V EM will be ~ 3V