Sol 47 TEGA Safe Mode

Time Line

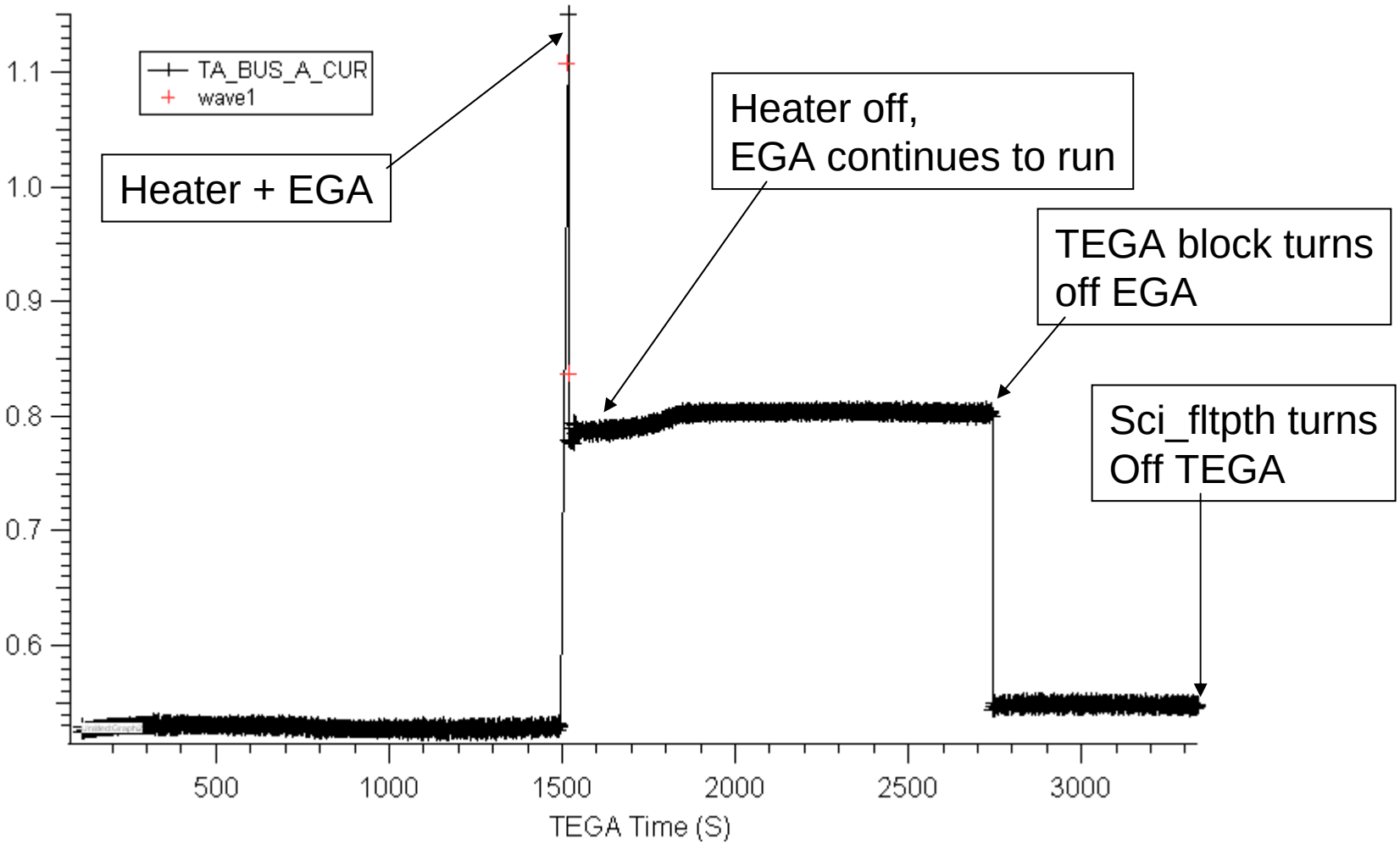
- 1516.783 (S/C time 900374596.779) – EGA commanded ON, EGA Heater goes ON
- 1518.000 – TEFSW receives corrupt engineering packet
- 1520.004 – EGA heater goes OFF
- 1535.733 – First EGA Boot Message
- 1578.033 – TEGA reports successful EGA startup

19 minutes later

- 2718.226 – EGA receives first power down command from our block
- 2743.212 – sci_fltpth issues TEGA shutdown

Corrupt Engineering Packet

- TEFSW does not check packet checksum
- Packet flagged with a checksum error on the ground
- Inspection of packet shows a normal 514 byte engineering packet, BUT
- The last 6 bytes were replaced by the VML_SET packet containing the GV_TEGA_EGA_ABOVE_MIN_OP_TEMP = 1 global variable command


TA_BUS_A_CUR
wave1
Heater + EGA
Heater off,
EGA continues to run
TEGA block turns
off EGA
Sci_fltpth turns
Off TEGA
1.1
1.0
0.9
0.8
0.7
0.6
500
1000
1500
2000
2500
3000
TEGA Time (S)

Corrupt Engineering Packet

Type 1
= engineering

```
0000000 0147 0202 7bdb 1600 b029 1700 4700 000e
0000010 0ab1 dc16 0002 420b b4dc 1600 0cad 2bb7
0000020 dc16 001a 0838 badc 1600 22a6 0bbe dc16
0000030 0023 400a c1dc 1600 2417 00c4 dc16 0000
0000040 0d0a 83e4 1600 0242 0b86 e416 000c ad2b
0000050 89e4 1600 1a12 388d e416 0022 9e0b 90e4
0000060 1600 233e 0a93 e416 0024 1900 96e4 1600
0000070 000d 0a55 ec16 0002 420b 58ec 1600 0cae
0000080 2b5b ec16 001a 0e38 5fec 1600 22c1 0b62
0000090 ec16 0023 3d0a 65ec 1600 2414 0068 ec16
00000a0 0000 0d0a 24f4 1600 0241 0b27 f416 000c
00000b0 ad2b 2af4 1600 1afd 372d f416 0022 ac0b
00000c0 31f4 1600 2345 0a34 f416 0024 1700 37f4
00000d0 1600 000d 0af6 fb16 0002 420b f9fb 1600
00000e0 0cae 2bfc fb16 001a 1038 00fc 1600 22a2
00000f0 0b03 fc16 0023 3f0a 06fc 1600 2416 0009
0000100 fc16 0000 0d0a c803 1700 0242 0bcb 0317
0000110 000c b02b ce03 1700 1a0e 38d2 0317 0022
0000120 ba0b d503 1700 233f 0ad8 0317 0024 1700
0000130 dc03 1700 000e 0a97 0b17 0002 420b 9a0b
0000140 1700 0cae 2b9d 0b17 001a fe37 a10b 1700
0000150 22b1 0ba4 0b17 0023 520a a70b 1700 2417
0000160 00aa 0b17 0000 0d0a 6913 1700 0242 0b6c
0000170 1317 000c b02b 6f13 1700 1a0b 3873 1317
0000180 0022 a50b 7613 1700 2342 0a79 1317 0024
0000190 1900 7d13 1700 000d 0a38 1b17 0002 410b
00001a0 3b1b 1700 0cb0 2b3e 1b17 001a 0f38 421b
00001b0 1700 22ba 0b45 1b17 0023 3c0a 481b 1700
00001c0 241a 004b 1b17 0000 0e0a 0a23 1700 0242
00001d0 0b0d 2317 000c b02b 1023 1700 1a02 3814
00001e0 2317 0022 b10b 1723 1700 2350 0a1a 2317
00001f0 0024 1600 1e23 1700 1610 27c7 095f 0100
0000200 0a5f
0000202
```

6 Byte VML_SET packet

How Can This Be?

- S/C communication hardware and software inherited from Odyssey GRS
  - TEGA has 2 S/C transmit buffers, and many packet assembly buffers
  - When a packet is fully assembled in one of the packet buffers a flag is set
  - Background loop sees the flag, checks for available S/C buffer
    - If no buffer available, do nothing
  - If buffer is available, packet is copied into buffer and buffer is marked BUSY
    - If transmitter is not busy, initiate buffer transmission
    - If transmitter is busy, do nothing

Meanwhile, in hardware land…

- DMA unit sends interrupt to 386 FSW when transmitter goes not busy
  - If there is data in a S/C buffer, 386 FSW sets a byte counter in the DMA unit
  - DMA unit goes busy and starts sending bytes from the buffer to the S/C

Possible Failure Mechanisms

- 386 FSW “forgets” that the engineering packet is being transmitted
  - Copies the VML_SET packet into the buffer while it is being transmitted
- FPGA “forgets” which buffer is being transmitted
  - Starts sending data from the other buffer before finishing the current buffer
- TEFSW is reading bytes out of the PACI
  - VML_SET packet arrives and somehow overwrites end of engineering packet